JP,10-108040,A

CLAIMS

[Claim(s)]
[Claim 1] In the gamma correction circuit for a liquid crystal device drive which carries out D/A conversion of the M bit digital display signal, and generates the analog driving signal of a liquid crystal device (61 - 6-N) the 1st and 2nd reference voltage means (V0, V64) -- this -- with the resistance (r1, r2, --, r64) of 2M piece by which series connection was carried out between the 1st and 2nd reference voltage means The gamma correction circuit for a liquid crystal drive characterized by having provided the decoder (33) which chooses one of the electrical potential differences of each node of said resistance according to said M bit digital display signal, and is made into said analog driving signal, and making the ratio of the value of said the resistance of each agree in the ratio of the gamma correction electrical potential difference of said liquid crystal device.
[Claim 2] said every -- the gamma correction circuit for a liquid crystal drive according to claim 1 where the 1st and 2nd reference voltage means possesses a voltage follower.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the gamma correction circuit for a liquid crystal drive in the liquid crystal equipment which can be displayed full color.
[0002]
[Description of the Prior Art] In recent years, the liquid crystal display is in the limelight as a flat panel display excellent in the display grace and responsibility of the liquid crystal itself, and is used for the liquid crystal projector which are a personal computer, a liquid crystal television, and its application product. From now on, the application side over the multimedia field which can display the image of both digital one and an analog will be expected.
[0003] Liquid crystal has the light transmittance property shown in drawing 3 . That is, light transmittance shows the nonlinear gamma property to liquid crystal applied voltage. In addition, drawing 3 is the case of the NOMA white mold liquid crystal containing active matrix liquid crystal.
[0004] In order to amend the gamma property shown in drawing 3 , the gamma correction circuit is prepared in a full color display, i.e., gradation control, of liquid crystal. As the relation of the gradation values 0, 1, and 2, --, 2M-1, and light transmittance which are obtained by this gamma correction circuit is shown in drawing 4 , a linearity property will be shown, and in a full color display, A is the brightest case at the time of the gradation

value 0, B is the brightest case at the time of gradation value 2M-1, it is only that correspondences of data differ, and the light transmittance property is the same.
[0005] Drawing 5 is the block circuit diagram showing a liquid crystal display including the conventional gamma correction circuit. In drawing 5 , the data register with which 1 incorporates the 6-bit digital display signals R, G, and B from the exterior, and 2 are latch circuits which latch a 6-bit digital signal synchronizing with strobe signal ST. 3 is a gamma correction circuit which consists of digital one / an analog (D/A) transducer of a juxtaposition N stage, it carries out D/A conversion of the 6-bit digital display signal of a latch circuit 2, supplies it to the voltage follower 4-1 of N stage - 4-N, and is impressed to a liquid crystal device 6-1 - 6-N through a switching element 5-1 - 5-N.
[0006] In the gamma correction circuit 3, reference voltage is generated by nine voltage followers 31-0 to 31-9, and the resistance ladder 32, and reference voltage is chosen by M->21 decoder 33 of N stage constituted by the ROM switch. In this case, each reference voltages V0-V8 of a voltage follower 31-0 to 31-8 are the reference voltages by which comma amendment was carried out, and correspond to the high order triplets D5, D4, and D3 of a digital display signal. As shown in drawing 6 , namely, V D5 D4 D3V8 0 0 0V7 0 0 1V6 0 1 0V5 0 1 1V4 1 0 0V3 1 0 1V2 1 1 0V1 1 1 It is 1.
[0007] Furthermore, between each voltage follower 31-0 - 31-N, series connection of eight equal resistance of the resistance ladder 32 is carried out, and reference voltage at equal intervals has occurred. In this case, the reference voltage generated by resistance of the resistance ladder 32 is the reference voltage by which Gance amendment was carried out in false, corresponds to the low order triplets D2, D1, and D0 of a digital display signal, and corresponds to the linearity property part of drawing 6 .
[0008] Thus, the electrical potential difference of nine pieces was given for 64 gradation of RGB each color precision of 6 bits from the exterior, and the full color display is realized by dividing between each of these electrical potential differences into the electrical potential difference of eight pieces at equal intervals, and performing the gamma correction by 64 false values (reference: NEC data sheet MOS IC muPD June, 1995 [16622 or]).
[0009]
[Problem(s) to be Solved by the Invention] However, in the gamma correction circuit shown in drawing 5 , it is only the true gamma correction electrical potential differences V0, V1, --, V8, and the remaining reference voltages have an error to a true gamma correction electrical potential difference, cannot perform the optimal gamma correction, but have the technical problem that the grace of a full color display falls. Moreover, in order to give the reference voltages V0, V1, --, V8 of nine pieces from the exterior, nine operational amplifiers are needed, and the technical problem that the rise of a manufacturing cost is caused also occurs.
[0010]
[Means for Solving the Problem] In the gamma correction circuit for a liquid crystal device drive which this invention carries out D/A conversion of the M bit digital display signal, and generates the analog driving signal of a liquid crystal device in order to solve an above-mentioned technical problem The resistance of 2M piece by which series connection was carried out between the 1st and 2nd reference voltage means, and these [1st] and the 2nd reference voltage means, The decoder which chooses one of the electrical potential differences of each node of resistance according to a M bit digital

display signal, and is made into said analog driving signal is provided, and the ratio of the value of each resistance is made to agree in the ratio of the gamma correction electrical potential difference of said liquid crystal device.
[0011]
[Embodiment of the Invention] Drawing 1 is the block circuit diagram showing a liquid crystal display including the gestalt of operation of the 1st of the gamma correction circuit concerning this invention. In drawing 1 , the voltage follower 31-1 to 31-7 in the gamma correction circuit of drawing 5 is not formed, and resistance ladder 32' which consists of resistance gamma1, gamma2, --, gamma64 of 64 (= 28) individuals is prepared among voltage follower 31-0 - 31-8. If it puts in another way so that the broken line of drawing 6 may turn into a curve, the value of the resistance gamma1, gamma2, --, gamma64 of resistance ladder 32' will be assigned so that a nonlinear electrical potential difference from which the permeability of the light of a liquid crystal device serves as a straight line can be generated. That is, the ratio of resistance gamma1 and gamma2, --, gamma64 value is made to agree in the ratio of a gamma correction electrical potential difference.
[0012] Drawing 2 is the block circuit diagram showing a liquid crystal display including the gestalt of operation of the 2nd of the gamma correction circuit concerning this invention. In drawing 2 , the voltage follower 31-0 to 31-8 in the gamma correction circuit of drawing 2 does not prepare. That is, in drawing 1 , although impedance of a reference supply was made low by the voltage follower 31-0 and 31-8, when a liquid crystal load is small and the write-in property of liquid crystal is stable, the voltage follower 31-0 to 31-8 of drawing 1 can be deleted.
[0013]
[Effect of the Invention] Since the ratio of each resistance of a resistance ladder was set up according to this invention so that a gamma correction electrical potential difference could be generated as explained above, a true gamma correction electrical potential difference can obtain, therefore grace of a full color display can be made high. Moreover, since a voltage follower can be decreased, a manufacturing cost can be reduced.
TECHNICAL FIELD

[Field of the Invention] This invention relates to the gamma correction circuit for a liquid crystal drive in the liquid crystal equipment which can be displayed full color.
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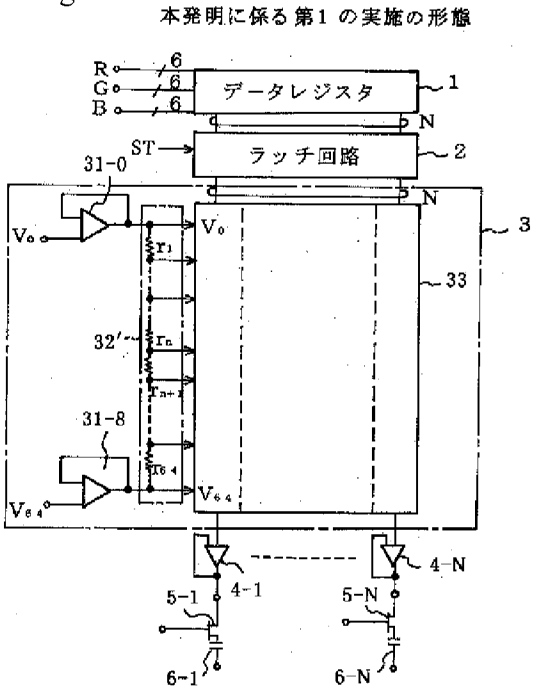
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block circuit diagram showing a liquid crystal display including the gestalt of operation of the 1st of the gamma correction circuit for a liquid crystal device drive concerning this invention.
[Drawing 2] It is the block circuit diagram showing a liquid crystal display including the gestalt of operation of the 2nd of the gamma correction circuit for a liquid crystal device drive concerning this invention.

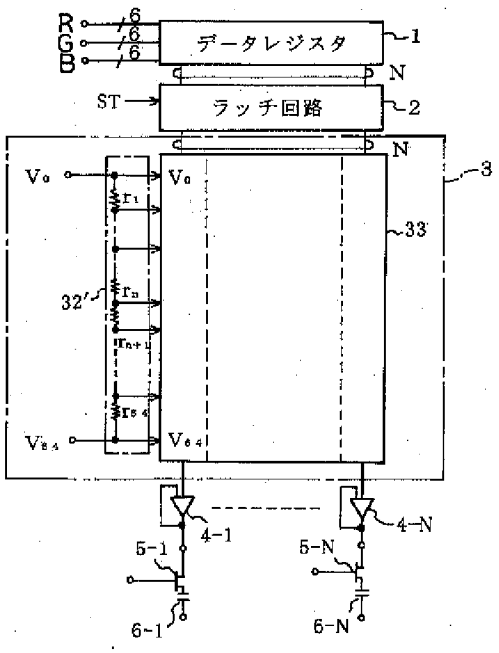
[Drawing 3] It is the graph which shows the light transmittance property of liquid crystal.
[Drawing 4] It is the graph which shows the light transmittance property of liquid crystal.
[Drawing 5] It is the block circuit diagram showing a liquid crystal display including the conventional gamma correction circuit for a liquid crystal device drive.
[Drawing 6] It is a graph explaining the electrical potential differences V0-V8 of drawing 5 .
[Description of Notations]
1 -- Data register
2 -- Latch circuit
3 -- Gamma correction circuit
31-0 to 31-8 -- Voltage follower
32 32' -- Resistance ladder
33 -- Decoder
4-1 - 4-N -- Voltage follower
5-1 - 5-N -- Switching element
6-1 - 6-N -- Liquid crystal device
Drawing 1



3 …ガンマ補正回路
31-0、31-8…電圧ホロワ
32′ …抵抗ラダー回路
33…デコーダ
4-1～4-N…電圧ホロワ
5-1～5-N…スイッチング素子
6-1～6-N…液晶素子

Drawing 2

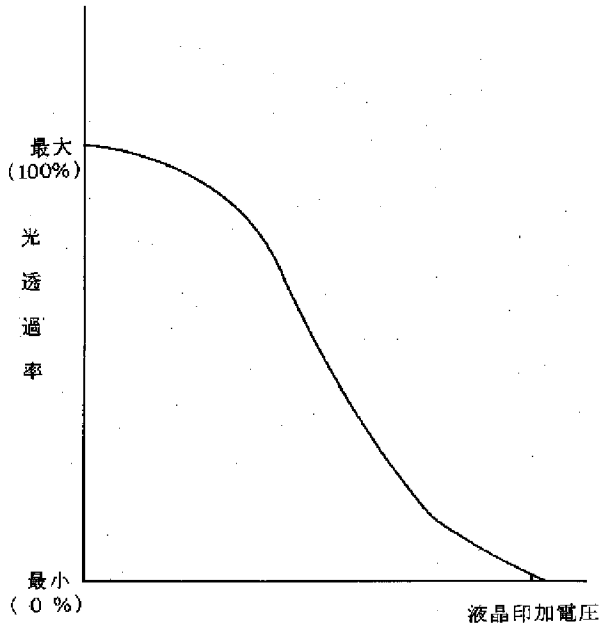
本発明に係る第2の実施の形態



3 …ガンマ補正回路
32′ …抵抗ラダー回路
33…デコーダ
4-1～4-N…電圧ホロワ
5-1～5-N…スイッチング素子
6-1～6-N…液晶素子

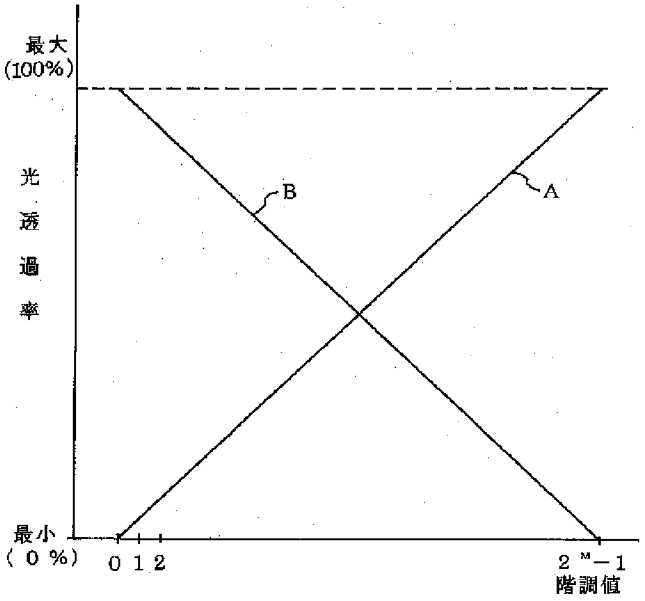
Drawing 3

液晶の光透過率特性（補正前）



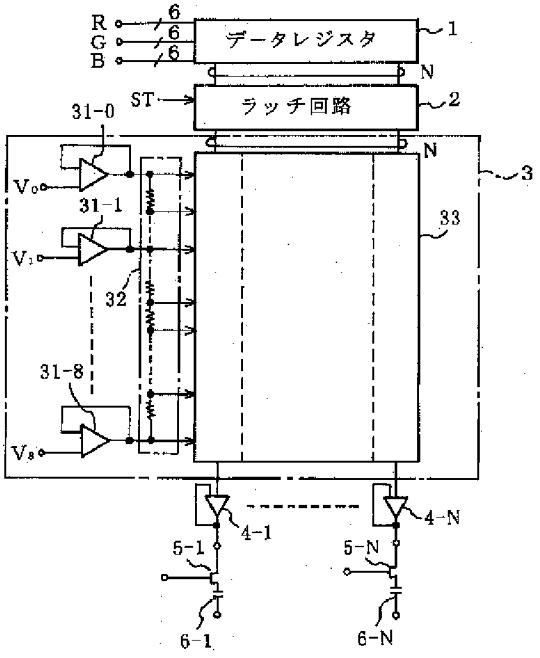
Drawing 4

液晶の光透過率特性（補正後）



Drawing 5

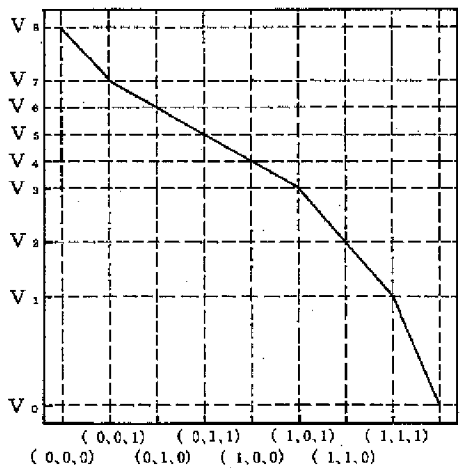
従来のガンマ補正回路を含む
液晶表示装置



3 …ガンマ補正回路
31-0、31-8…電圧ホロワ
32…抵抗ラダー回路
33…デコーダ
4-1～4-N…電圧ホロワ
5-1～5-N…スイッチング素子
6-1～6-N…液晶素子

Drawing 6

図5 の電圧Ｖ０ ～ Ｖ８を説明するグラフ



（Ｄ８、Ｄ４、Ｄ３）

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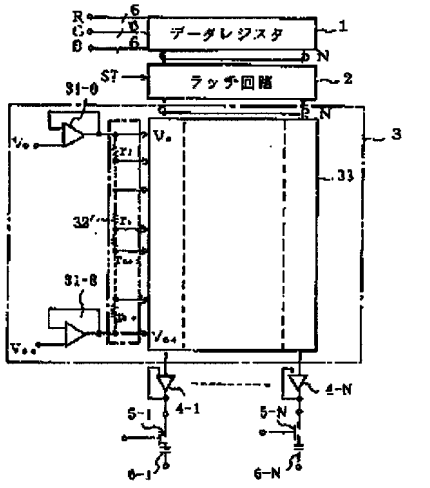
(54)【発明の名称】　液晶素子駆動用ガンマ補正回路

(57)【要約】

【課題】　真のガンマ補正電圧に対して誤差があり、最適なガンマ補正ができなかった。

【解決手段】　ラッチ回路２から６ビットディジタル信号をＤ／Ａ変換して液晶素子６－１～６－Ｎに供給するガンマ補正回路３は、基準電圧V_0，V_{64}を発生する電圧ホロワ３１－０，３１－８，基準電圧V_0、V_{64}を抵抗分圧する抵抗ラダー回路３２′、及びデコーダ３３よりなる。抵抗ラダー回路３２′の各抵抗γ_1，γ_2，…，γ_{64}の比は液晶素子６－１～６－Ｎのガンマ補正電圧の比に合致させた。

本発明に係る第１の実施の形態



3…ガンマ補正回路
31-0、31-8…電圧ホロワ
32′…抵抗ラダー回路
33…デコーダ
4-1～4-N…電圧ホロワ
5-1～5-N…スイッチング素子
6-1～6-N…液晶素子

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【特許請求の範囲】

【請求項１】　Ｍビットデジタル表示信号をＤ／Ａ変換して液晶素子（６１～６－Ｎ）のアナログ駆動信号を発生する液晶素子駆動用ガンマ補正回路において．

第１．第２の基準電圧手段（V_0，V_{2^M}）と．

該第１、第２の基準電圧手段間に直列接続された2^M個の抵抗（r_1，r_2，…，r_{2^M}）と．

前記Ｍビットデジタル表示信号に従って前記抵抗の各ノードの電圧のうち１つを選択して前記アナログ駆動信号とするデコーダ（３３）とを具備し．

前記各抵抗の値の比を前記液晶素子のガンマ補正電圧の比に合致させたことを特徴とする液晶駆動用ガンマ補正回路。

【請求項２】　前記各第１．第２の基準電圧手段が電圧ホロワを具備する請求項１に記載の液晶駆動用ガンマ補正回路。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はたとえばフルカラー表示が可能な液晶装置における液晶駆動用ガンマ補正回路に関する。

【０００２】

【従来の技術】近年、液晶表示装置は．液晶自体の表示品位及び応答性に優れたフラットパネル表示装置として脚光を浴びており、パーソナルコンピュータ、液晶テレビ．その応用製品である液晶プロジェクタ等に利用されている。今後．ディジタル．アナログ双方の画像を表示できるマルチメディア分野に対する応用面が期待されている。

【０００３】液晶は、図３に示す光透過率特性を有する。つまり、液晶印加電圧に対して光透過率は非線形であるガンマ特性を示している。なお．図３はアクティブマトリクス液晶をきむノーマホワイト型液晶の場合である。

【０００４】図３に示すガンマ特性を補正するために、液晶のフルカラー表示、すなわち、階調制御において、ガンマ補正回路が設けられている。このガンマ補正回路によって得られる階調値０．１，２，…，2^M-1と光透過率との関係は、図４に示すごとく．線形特性を示すことになり、フルカラー表示において．Ａは階調値０のときに最も明るい場合であり、Ｂは階調値2^M-1のときに最も明るい場合であり．データの対応が異なるのみで．光透過率特性は同一である。

【０００５】図５は従来のガンマ補正回路をきむ液晶表示装置を示すブロック回路図である。図５において、１は外部より６ビットディジタル表示信号Ｒ，Ｇ．Ｂを取り込むデータレジスタ、２はストローブ信号ＳＴに同期して６ビットディジタル信号をラッチするラッチ回路である。３は並列Ｎ段のディジタル／アナログ（Ｄ／Ａ）変換器よりなるガンマ補正回路であって、ラッチ回路２の６ビットディジタル表示信号をＤ／Ａ変換してＮ段の電圧ホロワ４－１～４－Ｎに供給し．スイッチング素子５－１～５－Ｎを介して液晶素子６－１～６－Ｎに印加する。

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【０００６】ガンマ補正回路３においては、９個の電圧ホロワ３１－０～３１－９及び抵抗ラダー回路３２によって基準電圧を発生し、ＲＯＭスイッチによって構成されるＮ段の2^M－１デコーダ３３によって基準電圧の選択を行う。この場合、電圧ホロワ３１－０～３１－８の各基準電圧V_0～V_8はガンマ補正された基準電圧であって．ディジタル表示信号の上位３ビットD_2，D_1，D_0に対応する。すなわち、図６に示すごとく、

V	D_2	D_1	D_0
V_0	0	0	0
V_1	0	0	1
V_2	0	1	0
V_3	0	1	1
V_4	1	0	0
V_5	1	0	1
V_6	1	1	0
V_7	1	1	1

である。

【０００７】さらに、各電圧ホロワ３１－０～３１－Ｎ間には、抵抗ラダー回路３２の８個の等しい抵抗が直列接続されており．等間隔の基準電圧が発生している。この場合、抵抗ラダー回路３２の抵抗によって発生する基準電圧は疑似的にガンス補正された基準電圧であって、ディジタル表示信号の下位３ビットD_2，D_1，D_0に対応し．また、図６の線形特性部分に対応する。

【０００８】このように．ＲＧＢ各色６ビット精度の６４階調を、外部より９個の電圧を与え．これらの各電圧間を８個の等間隔の電圧に分割して疑似的な６４値によるガンマ補正を行うことによりフルカラー表示を実現している（参照：ＮＥＣデータシートＭＯＳ集積回路μＰＤ１６６２２．１９９５年６月）。

【０００９】

【発明が解決しようとする課題】しかしながら．図５に示すガンマ補正回路においては、真のガンマ補正電圧V_0，V_1，…，V_8のみであり、残りの基準電圧は真のガンマ補正電圧に対して誤差を有し、この結果、最適なガンマ補正ができず、フルカラー表示の品位が低下するという課題がある。また、９個の基準電圧V_0，V_1，…，V_8を外部より与えるために９個のオペアンプを必要とし．製造コストの上昇を招くという課題もある。

【００１０】

【課題を解決するための手段】上述の課題を解決するために本発明は．Ｍビットデジタル表示信号をＤ／Ａ変換して液晶素子のアナログ駆動信号を発生する液晶素子駆動用ガンマ補正回路において、第１．第２の基準電圧手段と．これら第１、第２の基準電圧手段間に直列接続さ

れた2"個の抵抗と、Mビットデジタル表示信号に従って抵抗の各ノードの電圧のうち1つを選択して前記アナログ駆動信号とするデコーダとを具備し、各抵抗の値の比を前記液晶素子のガンマ補正電圧の比に合致させたものである。

【００１１】

【発明の実施の形態】図１は本発明に係るガンマ補正回路の第１の実施の形態を含む液晶表示装置を示すブロック回路図である。図１においては、図５のガンマ補正回路における電圧ホロワ３１－１～３１－７は設けず、また、電圧ホロワ３１－０～３１－８間には、６４（＝２⁶）個の抵抗r_1、r_2、…、r_{64}よりなる抵抗ラダー回路３２'が設けられている。抵抗ラダー回路３２'の抵抗r_1、r_2、…、r_{64}の値は、図６の折線が曲線となるように、言い換えると、液晶素子の光の透過率が直線となるような非線形電圧を発生できるように、割り当てる。すなわち、抵抗r_1、r_2、…、r_{64}値の比をガンマ補正電圧の比に合致させる。

【００１２】図２は本発明に係るガンマ補正回路の第２の実施の形態を含む液晶表示装置を示すブロック回路図である。図２においては、図２のガンマ補正回路における電圧ホロワ３１－０～３１－８は設けない。すなわち、図１においては、電圧ホロワ３１－０、３１－８によって基準電源のインピータンスを低くしていたが、液晶負荷が小さくかつ液晶の書込み特性が安定している場合には、図１の電圧ホロワ３１－０～３１－８を削除できる。

【００１３】

＊【発明の効果】以上説明したように本発明によれば、抵抗ラダー回路の各抵抗の比をガンマ補正電圧を発生できるように設定したので、真のガンマ補正電圧が得ることができ、従って、フルカラー表示の品位を高くできる。また、電圧ホロワを減少できるので、製造コストを低減できる。

【図面の簡単な説明】

【図１】本発明に係る液晶素子駆動用ガンマ補正回路の第１の実施の形態を含む液晶表示装置を示すブロック回路図である。

【図２】本発明に係る液晶素子駆動用ガンマ補正回路の第２の実施の形態を含む液晶表示装置を示すブロック回路図である。

【図３】液晶の光透過率特性を示すグラフである。

【図４】液晶の光透過率特性を示すグラフである。

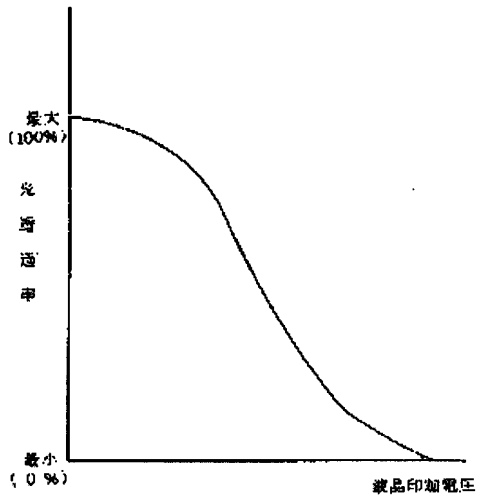
【図５】従来の液晶素子駆動用ガンマ補正回路を含む液晶表示装置を示すブロック回路図である。

【図６】図５の電圧V_0～V_9を説明するグラフである。

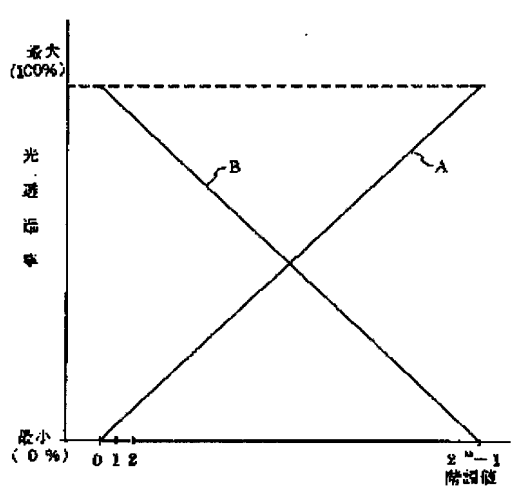
【符号の説明】

１…データレジスタ
２…ラッチ回路
３…ガンマ補正回路
３１－０～３１－８…電圧ホロワ
３２、３２'…抵抗ラダー回路
３３…デコーダ
４－１～４－Ｎ…電圧ホロワ
５－１～５－Ｎ…スイッチング素子
６－１～６－Ｎ…液晶素子

【図３】

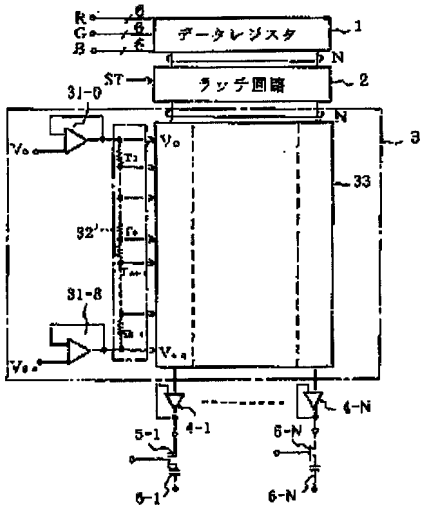


【図４】



【図１】

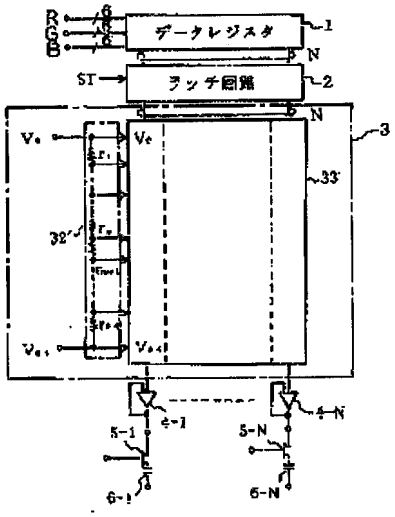
本発明に係る第1の実施の形態



3 …ガンマ補正回路
31-0、31-8…電圧ホロワ
32′ …抵抗ラダー回路
33…デコーダ
4-1～4-N…電圧ホロワ
5-1～5-N…スイッチング素子
6-1～6-N…液晶素子

【図２】

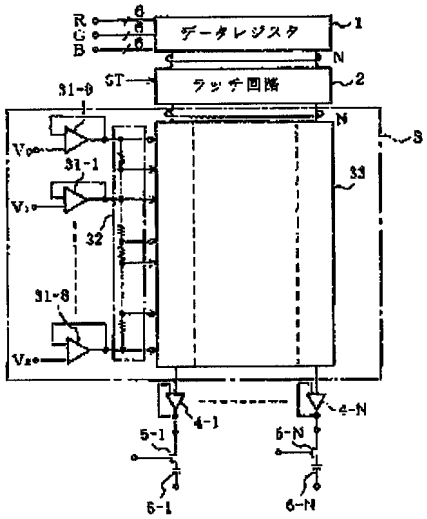
本発明に係る第2の実施の形態



3 …ガンマ補正回路
32′ …抵抗ラダー回路
33…デコーダ
4-1～4-N…電圧ホロワ
5-1～5-N…スイッチング素子
6-1～6-N…液晶素子

【図５】

従来のガンマ補正回路を含む液晶表示装置



3 …ガンマ補正回路
31-0、31-8…電圧ホロワ
32…抵抗ラダー回路
33…デコーダ
4-1～4-N…電圧ホロワ
5-1～5-N…スイッチング素子
6-1～6-N…液晶素子

【図６】

図5の電圧V₀ ～ V₄を説明するグラフ